FORM PTO-1390 (REV 12-2001) US DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

Agent's Docket No. **FP01074US**

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

U.S. APPLICATION NO. (If known, see 37 CFR 1.5) 10/049486 NONE

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT Appl. No.: PCT/CN00/00068	**March 29, 2000**	**August 30, 1999**

TITLE OF INVENTION

PARALLEL PLATE DIODE

APPLICANT(S) FOR DO/EO/US

YELIN XU ET AL.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [ ] This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. [ ] The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [ ] is attached hereto (required only if not communicated by the International Bureau).
   b. [X] has been communicated by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [X] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. [X] is attached hereto.
   b. [ ] has been previously submitted under 35 U.S.C. 154(d)(4).
7. [ ] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. [ ] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] An English lanugage translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. [X] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [ ] A FIRST preliminary amendment.
14. [ ] A SECOND or SUBSEQUENT preliminary amendment.
15. [ ] A substitute specification.
16. [ ] A change of power of attorney and/or address letter.
17. [ ] A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. [ ] A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. [ ] A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. [ ] Other items or information:

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Bonnie Lee

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U.S. APPLICATION NO. (If known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	Agent's Docket No.
10/049486	PCT Appl. No.: PCT/CN00/00068	FP01074US

21. [ ] The following fees are submitted:	CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5): Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1040.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO .... **$890.00** International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$740.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$710.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$1040.00	
Surcharge of **$130.00 for furnishing the oath or declaration later than [ ] 20 [ ] 30 Months from the earliest claimed priority date (37 CFR 1.492(e)).**	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	18 -20 =	0	X $18.00	$0.00	
Independent Claims	1 -3 =	0	X $84.00	$0.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $280.00	$280.00	
TOTAL OF ABOVE CALCULATIONS				$1320.00	
[ ] Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.			+	$660.00	
SUBTOTAL =				$660.00	
Processing fee of **$130.00** for furnishing the English translation later than [ ] 20 [ ] 30 **Months from the earliest claimed priority date (37 CFR 1.492(f)).**				$	
TOTAL NATIONAL FEE =				$660.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +					
TOTAL FEES ENCLOSED =				$660.00	
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NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive) 37 CFR 1.137 (a) or (b) must be filed and granted to restore the application to pending status.

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41,088
REGISTRATION NUMBER

FP01074US

IN THE US PATENT AND TRADEMARK OFFICE

US Application Number:	Not Yet Assigned
US Filing Date	February 9, 2002
International Application Number:	PCT/CN00/00068
International Filing Date:	March 29, 2000
Agent's Docket Number:	FP0174US
Applicants:	Yelin Xu, et al.
Application Title:	Parallel Plate Diode
Examiner:	Not Yet Assigned
Art Unit:	Not Yet Assigned

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AMENDMENT

Commissioner of Patents and Trademarks
Washington, DC 20231

Sir:
Prior to examination of the above PCT U.S. National Stage application, kindly amend the application as follows.

CLAIMS:
Kindly amend claims **11**, **13**, **17**, and **18** by entering the clean version of the claims shown on the replacement claim page below. The changes to the claims are shown in the accompanying "Version with Markings to Show Changes Made".

REPLACEMENT CLAIMS **11, 13, 17, 18**

11. The parallel plate diode according to claim 1, wherein said metal electrode is made by kovar-alloy.

13. The parallel plate diode according to claim 1, wherein there are recesses on the surface where the two metal electrodes that make up the parallel plate diode contact the semiconductor material, wherein average diameter of the recesses on one side is equal to or smaller than 0.7 micrometer while the average diameter of the recesses on the other side is bigger than 0.7 micrometer.

17. The parallel plate diode according to claim 1, wherein said semiconductor material is liquid semiconductor material.

18. The parallel plate diode according to claim 1, wherein said semiconductor material is high resistance metal alloy.

AMENDED CLAIMS 11, 13,17, 18

Version With Markings To Show Changes Made

11. The parallel plate diode according to claim 1 **[or 2]**, wherein said metal electrode is made by kovar-alloy.

13. The parallel plate diode according to claim 1 **[or 2]**, wherein there are recesses on the surface where the two metal electrodes that make up the parallel plate diode contact the semiconductor material, wherein average diameter of the recesses on one side is equal to or smaller than 0.7 micrometer while the average diameter of the recesses on the other side is bigger than 0.7 micrometer.

17. The parallel plate diode according to claim 1 **[or 13]**, wherein said semiconductor material is liquid semiconductor material.

18. The parallel plate diode according to claim 1 **[or 13]**, wherein said semiconductor material is high resistance metal alloy.

REMARKS:

CLAIM AMENDMENTS

To expedite prosecution, the Applicants have amended the claims to be more consistent with U.S. patent practice. Specifically, the Applicants have removed the multiple dependencies from claims **11**, **13**, **17**, and **18**. The Applicants submit that no new matter has been entered with these amendments. Furthermore, the Applicants submit that the minor changes introduced with this amendment do not narrow any of the claims within the meaning of the decision in *Festo Corporation v. Shoketsu Kinzoku Kogyo Kabushiki Co., Ltd* (234 F.3d 558).

REQUEST FOR REFUNED OF MULTIPLE DEPENDENT CLAIM FEE

The Applicants submit that since there are no longer any multiple dependent claims in the application, the multiple dependent claim charge no longer applies. Therefore, the Applicants respectfully request a refund of the multiple dependent claim fee of $140 submitted at the time of filing of the application.

CONCLUSION

In view of the above amendments and remarks, the Applicants respectfully request that the Examiner consider the application and point out the allowable subject matter in the next Office Action.

Respectfully submitted,

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Patent Agent, Reg. No. 41,088

Date: 2/28/2007

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Parallel Plate Diode

Field of Invention

The present invention relates to a semiconductor device, particularly to a parallel plate diode.

Description of Background art

The conventional semiconductor diodes has an p-n junction structure made of semiconductor materials in which the carriers make orientated movements when extra electric field force is applied and they exhibit unidirectional conductivity. Such semiconductor diodes are mainly used as rectifying or switching device. Evidently, when no bias voltage or bias current is applied, the unidirectional conductivity of such diodes will disappear and become ordinary linear devices. There is another semiconductor device called selenium pile, made of several plate-like semiconductor materials --- selenium rectifying plate in parallel connection. It is a rectifying device that exhibits unidirectional conductivity only when extra electric field exists.

Summary of the Invention

An object of the present invention is to provide a parallel plate diode that can maintain unidirectional conductivity in the circuit with no application of bias voltage or bias current.

In order to accomplish the object mentioned above, a parallel plate diode comprising metal electrodes and semiconductor materials contacting metal electrodes, wherein the two thin plate electrodes made of metal are disposed in parallel, and a layer of thin plate semiconductor material sandwiched between the two thin plate electrodes. The concentration of the carriers in the semiconductor material layer is 20% or less than that of the electrons in the metal. One of the metal electrodes is made so as to have a plurality of recesses from its surface into the interior on the side that faces the semiconductor coat layer. The diameter of those

recesses is less than 4 micrometers.

Preferably, said recesses are well-shape cavities.

The parallel plate diode according to the present invention can be used as the detecting diode, which can improve the performance of the radiodetector. Furthermore, it can also be used as an electronic watch, a micro calculator as well as the power of other small power electric appliances.

Brief description of the drawings

The invention will be better understood by referring to the following description in conjunction with the figures, in which:

Figs. 1(a) and (b) show the unidirectional conductivity of the parallel plate diode with no bias voltage or bias current according to the present invention;

Fig. 2 is a sectional view of the structure of the "electric well" formed in the parallel plate diode according to the present invention;

Figs. 3(a)-(f) is a sectional of the recesses within the parallel plate diode of the present invention;

Fig. 4 is a sectional view of the structure of the well cavity of the well wall made of different material in the parallel plate diode of the present invention;

Figs. 5(a)-(d) are section views of the parallel plate diode of the present invention, in which 5(b) and (c) show that there are well-shape cavities within both of the metal electrodes of the diode;

Figs. 6(a) and (b) are diagrams showing the structure of the parallel plate diode according to preferred embodiment of the present invention, in which Fig. 6(a) shows the section structure and 6(b) is a top view of the invention.

Figs. 7(a) and (b) is a microscopic view of the structure of the diode according to the preferred embodiment of the present invention, in which Fig. 7(a) is a sectional view and Fig. 7(b) is a top view of the diode.

Fig. 8 is a testing curve of the experiment of the embodiment shown in Figs. 6(a) and (b).

Figs. 9(a) and (b) show the structure of the parallel plate diode according to another embodiment of the present invention, in which Fig. 9(a) is a front view and

Fig. 9(b) a top view.

Fig. 10 is a microscopic view of the structure of the embodiment shown in Figs. 9(a) and (b).

Fig. 11 is a testing curve of the experiment of the embodiment shown in Figs. 9(a) and (b).

Description of Preferred Embodiments

As shown in Figs. 1(a) and (b), when the parallel plate diode in the present invention are connected in closed loop circuit, there will be a continuous and constant direct current I_T flowing through the loop circuit. As shown in Fig. 2, when the recesses in the interior of the metal, such as the diameter of the well-shape cavity is small enough (less than 4 micrometers), the electrostatic attraction between the dissociated electrons bound by the metal crystal lattice on the surface of the well-shape cavity and their corresponding positive ions will be evidently displayed. Under the electrostatic pull, said positive ions and the electrons tend to be attached to the surface of the well-shape cavity, thus forming the internal electric filed E in the well. Then the conducting electrons on the surface of the other thin metal plate electrode in the above mentioned diode and on the bottom of the well will be gathered on the wall of the well under the warping force of the electric field E. The well cavity exhibits the effect of "more in, less out", thus forming an "electrons well". The parallel plate diode having said structure has non-bias unidirectional conductivity, namely, it can exhibit unidirectional electric current with no application of bias voltage and bias current because of the heat movement of the conducting electrons.

The distribution of the heat movement of the conducting electrons in the metal electrodes of the parallel plate diodes approximately satisfies the Maxwell equation distribution. Due to this, experiments show that the output voltage of the parallel plate diodes varies in a considerable range with the value of load, with a maximum of several hundred milli-volts. Experiments also show that when the output voltage is approximately 30 milli-volts, the corresponding output power is relatively big and

this corresponds to the mean speed of the heat movement of the conducting electrons.

The output current of the parallel plate diode in the present invention relate to the diameter of the well-shape cavity and the number of cavities in the electrodes. Specifically, when the diameter of the well cavity decreases, the unidirectional coefficient K of the diode increases and maintains the magnification of the electric current in the circuit. Furthermore, the more the well-shape cavities, the greater current the circuit will able to be maintain. It is feasible that the diameter of the well-shape cavity is approximately equal to the depth of the cavity. The applicant of the present invention has tried to study the relation between the diameter of the well cavity and the density of said electric current I_T from a purely theoretical approach, by pure experimentation as well as by experimentation with theory respectively and has achieved an approximate result. The result used in the description of the present invention is derived from experimentation with theory. For example, taking in consideration the silicon parallel plate diode having the above mentioned structure, when the output voltage is 30 milli-volts, according to analysis from experimentation the density I_T (ampere/**cm2**) of the output current has the following relation with the diameter D1 of the well-shape cavity:

$$I_T = K_3(\frac{K_4}{D_1})^{K_5} = 800(\frac{0.8\times10^{-6}}{D_1})^{4.9} \qquad (1)$$

where the unit of the diameter of the well cavity is centimeter and K3, K4, and K5 are all experimental coefficients. According to equation (1), the smaller the diameter of the well cavity, the more density the electric current. A diameter of 0.7 micrometer of the well cavity can be achieved in present invention. The output current of the parallel plate diode of present invention is 0.2 microampere. When the diameter of the well cavity is made 80Å by using the electron beam etching method, which will be discussed later, the present diode can maintain an output electric current whose density is as much as 800 amperes/cm2, which has a promising prospect in application.

Figs. 6(a), (b) and 7(a), (b) show parallel plate diodes made on the glass substrate 31, which is a 25 by 25 millimeters square glass plate with a thickness of 1.2 millimeter. The glass substrate has a chromium electrode 3 plated on it, and electrode 1 is made of antimony. The silicon layer 2 shown in the drawing is sandwiched between the above-mentioned chromium electrode 3 and the antimony electrode 1.

The different layers of the present embodiment can be made through coating by evaporation, in particular, the well-shape cavity can be formed through coating by evaporation or by electron beam etching. By coating of evaporation, the vacuum degree of the electrodes 1 and 3 being evaporated is $5*10^{-3}$Pa, and the vacuum degree of the silicon layer 2 being evaporated is 1.5-1.8Pa in the nitrogen environment. At this time, the diameter of the well-shape cavity formed is 0.7 micrometer with a depth of approximately 0.2 micrometer. The resulting chromium electrode 3 under such a condition is a smooth electrode as the positive pole of the diode, while the antimony electrode 1 is an electrode having a well-shape cavity as the negative pole of the diode.

In order to achieve a well-shape cavity with a diameter of 200 Å and a depth of 200 Å, a chromium layer 3 should first be coated by evaporation using the method of electron beam etching, then a cavity is carved on the chromium layer. The silicon layer 2 is formed by chemical vapor deposition. The antimony layer 1 is also formed through coating by evaporation. The vacuum degree of the chromium 3 and the antimony 1 should be maintained at $5*10^{-3}$Pa when being coated by evaporation.

Fig. 8 is the testing curve of the parallel plate diode of the present embodiment made by the method of coating by evaporation. When the diode of the present embodiment is connected in the circuit, as shown in Fig. 1(b), whose load is 3 mega ohms, at this time, the metal electrode that has the well-shape cavity is the negative pole and the other plate metal electrode is the positive pole. Fig. 8 shows simultaneously the output current and voltage achieved through such a method, in which the abscissa is the measuring time (the unit is minute) and the ordinate indicates the output voltage and current of the diode using the units of milli-volt and

ampere respectively. It can be seen from the Fig. 8 that the parallel plate diode of the embodiment of the present invention can obtain a stable output of voltage and current and a good performance of unidirectional conductivity.

The cross section of the diode of the embodiment of the present invention can be a circular, a square, rectangle or an irregular curve. As shown in Fig. 3(a)-(c), it can also be in a slot and these recesses fill the electrodes.

Said well cavity can also be in the form of an array of projections in which convex portions and concave portions are staggered each other, as shown in Fig. 3(e).

The silicon material used in the embodiment of the present invention can be n-type or p-type silicon, including high-resistance type, medium-resistance type, low-resistance type, mixed type or essential type silicon. And various kinds of germanium material or any kind of semiconductor material can be used to make the diode of the embodiment in the present invention. The metal electrode can be any homogeneous metal or alloy as long as it can fix the three layers of materials labeled 1, 2, and 3 as shown in Fig. 6 tightly together. Parallel plate diode made of these materials in the embodiment of the present invention can also achieve electric current and voltage output.

Furthermore, according the results of the abovementioned experiments, it is not difficult to understand for the person skilled in the art that liquid semiconductor materials, high resistance metal alloy can both serve as very efficient materials for the parallel plate diode, in which high-resistance alloy belongs to metal, whose intensity is much higher than semiconductors. When liquid semiconductor materials or high resistance metal alloy are used to make parallel plate diode, it can be very firm. As for the liquid materials, because of their mobility, the advantage of using them in making diodes lies in that once the diodes are damaged, it can be automatically repaired and that components made of such liquid materials are not subject to damage because of the difference in the expansion coefficients. Furthermore, liquid materials also have the advantage of good performance in heat exchange.

With the parallel plate diode having the abovementioned structure as a unit on

the substrate of the same glass or other insulators, the metal electrode having the well-shape cavity of each diode is coupled to the germanium electrode of the adjoining diode having the same structure, thus forming a parallel plate diode in series structure.

Only the diodes should be kept parallel to each other, and there is no restriction on the overall shape formed by said different layers. That is to say, the parallel plate in the present invention should not be restricted to the pure notion of a "parallel plate" of the "flat plate" type. In fact, Fig 5(a)-(d) is parallel plate structure.

It is noted that it is very difficult to achieve an electrode with an ideally smooth surface. In practice, there are recesses on the surface where the two metal electrodes that make up the parallel plate diode of the embodiment of the present invention contact the semiconductor material. The average diameter of the recesses on one side is equal to or smaller than 0.7 micrometer while the average diameter of the recesses on the other side is bigger than 0.7 micrometer. When such diode is connected in the closed circuit, the metal electrode whose recesses have smaller diameters is the negative pole, whereas the metal electrode whose recesses have bigger diameters is the positive pole. In general, the special contacting surface between the two electrodes and the semiconductor is filled with recesses with different depths and shapes. Such diodes can also output currents and volt.

The two walls of the well-shape cavity of the parallel plate diode of the present invention can be made of two substances, as shown in Fig. 4. If we use $e\Phi 1$ and $e\Phi 3$ respectively to represent the power function of the two walls of the well cavity, therefore, when they satisfy the following relation:

$$\Phi_1 < \Phi_3$$

The parallel plate diode on the well cavity of the well walls made of different substances will have good unidirectional coefficients. In particular, when such wall structure of the well cavity containing different materials is applied to the groove-shaped structure in Fig. 3(f), that is, both the right and the left sides of the groove are made of two kinds of materials and their power function meet the abovementioned relation, then a parallel plate diode having bigger output current

and higher voltage and high unidirectional coefficient can be achieved. Besides, the groove-shaped structure in Fig. 3(f) is easy for processing.

Figs. 9(a), (b) and 10 show another embodiment of the parallel plate diode according to the present invention, which uses kovar-alloy as the substrate.

As shown in Figs. 9(a) and (b), kovar-alloy whose heat expansion coefficient is about $3.1*10^{-6}$ is chosen to make a 20*20 millimeter metal substrate 3 whose thickness is 0.2 millimeter. There is a silicon layer 2 on the metal substrate with a total thickness of 2 micrometers and said silicon layer 2 forms continuous projections with the side opposite to the surface of the metal plate to which the said silicon layer 2 is attached (see Fig. 10) and the surface of such continuous projections contact the kovar-alloy electrode 1 made of another layer of kovar-alloy, thus the continuous projecting surface of the said silicon layer causes the latter kovar-alloy electrode 1 to form well-shape cavities.

In Fig. 10, label 2-2 indicates the first silicon layer plated by the lower vacuum layer 16 formed through coating by evaporation (in a nitrogen environment, the air pressure is maintained between1.5-1.8Pa), whereas label 2-1 indicates the second silicon layer formed by higher vacuum (about $5*10^{-3}$Pa) silicon filming, including 6 layers of silicon films to enhance the intensity of the plated films.

Fig. 11 shows the testing curves of the diode in the embodiment of the present invention. When the diode of the present embodiment is connected in the circuit, as shown in Fig. 1(b), whose load is 3 mega ohms, at this time, the metal electrode that has the well-shape cavity is the negative pole and the other thin plate metal electrode is the positive pole. Fig. 11 shows simultaneously the output current and voltage achieved through such a method, in which the abscissa is the measuring time (the unit is minute) and the ordinate indicates the output voltage and current of the diode using the units of milli-volt and ampere respectively. It can be seen that the use of the parallel plate diode of the embodiment of the present invention can assure a stable output of voltage and current and a good performance of unidirectional conductivity.

The parallel plate diode having the abovementioned structure can be taken as a

unit, each of the kovar-alloy electrodes having well-shape cavities of such diodes can join the kovar-alloy substrate of the other diode having identical structure so that they form a parallel plate diode in series.

What is claimed is:

1.A parallel plate diode, comprising:

metal electrodes and semiconductor materials contacting said metal electrodes, wherein the two thin plate electrodes made of metal disposed in parallel, and a layer of thin plate semiconductor material sandwiched between the two thin plate electrodes, the concentration of the carriers in the semiconductor material layer is 20% or less than that of the electrons in the metal, one of the metal electrodes is made so as to have a plurality of recesses from its surface into the interior on the side that faces the semiconductor coat layer, the diameter of those recesses is less than 4 micrometers.

2. The parallel plate diode according to claim 1, wherein said recesses are well-shape cavities.

3. The parallel plate diode according to claim 2, wherein said cross section of the well-shape cavity is a circular, a square, rectangle or an irregular curve.

4. The parallel plate diode according to claim 2, wherein said cross section of the well-shape cavity is groove-shape.

5. The parallel plate diode according to claim 2, wherein said cross section of the well-shape cavity is in the form of an array of projections in which convex portions and concave portions are staggered each other.

6. The parallel plate diode according to previously any one of claims, wherein said two walls of the well-shape cavity or groove-shape are made of two substances, eΦ1 and eΦ3 respectively represent the power function of the two walls of the well cavity, they satisfy the following relation:

$$\Phi_1 < \Phi_3$$

7. The parallel plate diode according to claim 1, wherein said substance between said metal electrodes is a substance of weak conductivity.

8. The parallel plate diode according to claim 1, wherein said parallel plate diode is attached to the insulated substrate.

9. The parallel plate diode according to claim 8, wherein said parallel plate

diode is attached to glass substrate.

10. The parallel plate diode according to claim 9, wherein said the metal electrode having the well-shape cavity of each diode is coupled to the germanium electrode of the adjoining diode having the same structure, thus forming a parallel plate diode in series structure.

11. The parallel plate diode according to claim 1 or 2, wherein said metal electrode is made by kovar-alloy.

12. The parallel plate diode according to claim 11, wherein said each of the kovar-alloy electrodes having well-shape cavities of such diodes can join the kovar-alloy substrate of the other diode having identical structure so that they form a parallel plate diode in series.

13. The parallel plate diode according to claim 1 or 2, wherein there are recesses on the surface where the two metal electrodes that make up the parallel plate diode contact the semiconductor material, wherein average diameter of the recesses on one side is equal to or smaller than 0.7 micrometer while the average diameter of the recesses on the other side is bigger than 0.7 micrometer.

14. The parallel plate diode according to claim 13, wherein said the surface of the two electrodes have recesses with different depths.

15. The parallel plate diode according to claim 13, wherein said the surface of the two electrodes have recesses with different shape.

16. The parallel plate diode according to claim 1, wherein said layers of materials are parallel to each other, there is no restriction on the overall shape formed by said different layers.

17. The parallel plate diode according to claim 1 or 13, wherein said semiconductor material is liquid semiconductor material.

18. The parallel plate diode according to claim 1 or 13, wherein said semiconductor material is high resistance metal alloy.

Abstract

A parallel plate diode comprising metal electrodes and semiconductor materials layer contacting said metal electrodes. Two thin plate electrodes made of metal are disposed in parallel, and there is a layer of thin plate semiconductor material sandwiched between the two thin plate electrodes, the concentration of the carriers in the semiconductor material layer is 20% or less than that of the electrons in the metal. One of the metal electrodes is made so as to have a plurality of recesses from its surface into the interior on the side that faces the semiconductor coat layer, the diameter of those recesses is less than 4 micrometers. These recesses are well-shape cavities and an array of the convex portions and concave portions are staggered each other. The cross section of the well shape is circular, square or rectangle. This diode output a current and a voltage in a closed loop circuit without bias voltage or bias current.

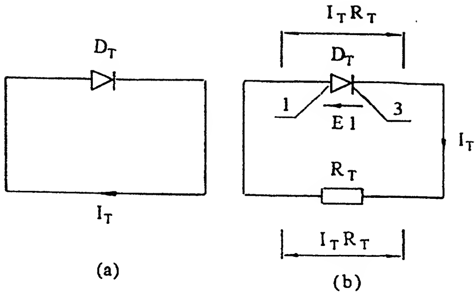


Fig.1

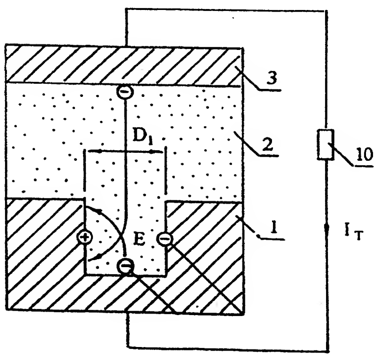


Fig.2

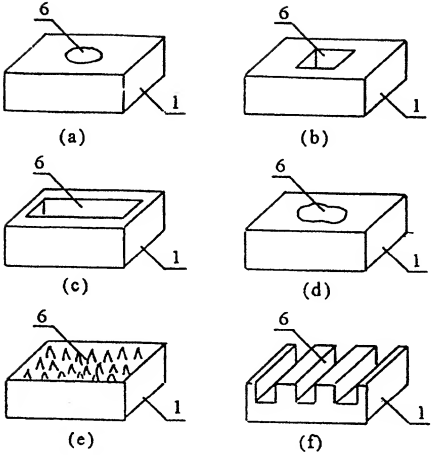


Fig.3

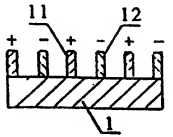


Fig.4

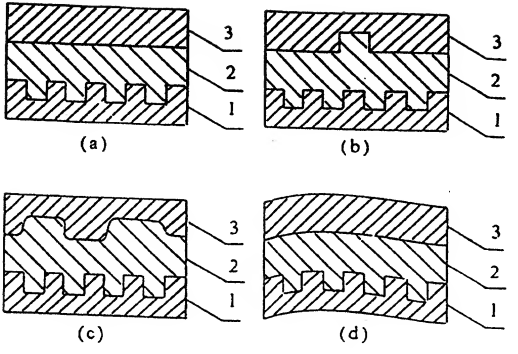


Fig.5

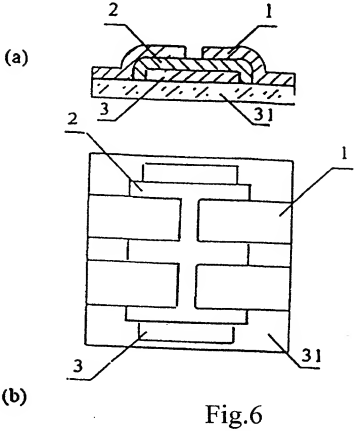
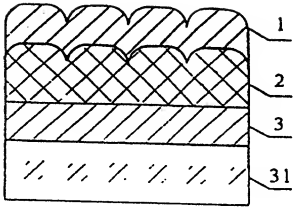
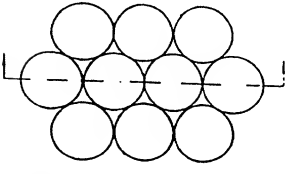


Fig.6



(a)



(b)

Fig.7

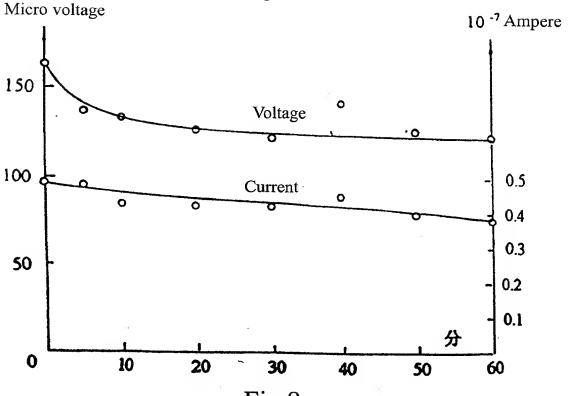


Fig.8

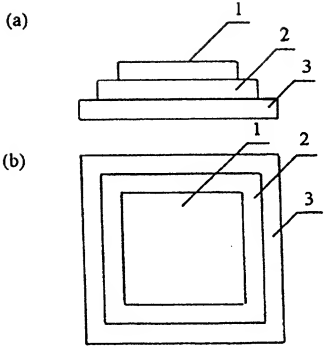


Fig.9

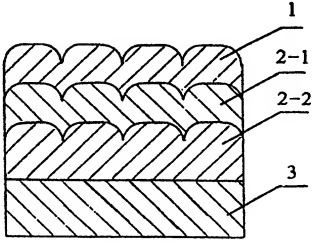


Fig.10

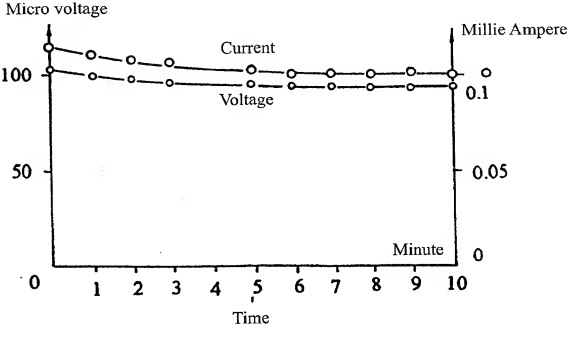


Fig.11

Agent Docket: FP01074US

Declaration for Patent Application

As a below named inventor, I hereby declare that my residence, post office address, and citizenship are as stated below next to my name, and that I believe I am the original, first and sole inventor (if only one is listed) or an original, first and joint inventor (if plural names are listed) of the subject matter which is claimed and for which a patent is sought on the invention described in application **PCT Appl. No.: PCT/CN00/00068** filed **March 29, 2000** entitled **Parallel Plate Diode** and any preliminary amendment filed concurrently herewith.

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	Residence:			
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Fifth Joint Inventor	Full name:		Citizenship:	
	Residence:			
	Postal Address:	**same as above**		

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a). I claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

PRIOR FOREIGN APPLICATION(S)

Country	Application Number	Date of Filing	Priority Claimed Under 35 U.S.C. §119
PR China	**99118929.9**	**August 30, 1999**	[ ] Yes [ ] No

I claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

PRIOR U. S. APPLICATION(S)

Application No	Filing Date	Status			
NONE		[ ] Provisional	[ ] Patented	[ ] Pending	[ ] Regular

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Title 18, §1001 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

INVENTOR SIGNATURE(S)

Yelin Xu — Feb. 5, 2002
YELIN XU — Date

Ling Jiang — Feb. 5, 2002
LING JIANG — Date

Qiang Xu — Feb. 5, 2002
QIANG XU — Date